APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/831,505	08/01/2001	Toru Aoki	2001-0565A	5693

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EXAMINER
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ART UNIT	PAPER NUMBER
2133	

DATE MAILED: 08/25/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE _3_ MONTH(S) FROM
THE MAILING DATE OF THIS COMMUNICATION.
- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) ☒ Responsive to communication(s) filed on _06 August 2004_.

2a) ☐ This action is **FINAL**.   2b) ☒ This action is non-final.

3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4) ☒ Claim(s) _1-3_ is/are pending in the application.

    4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5) ☐ Claim(s) _____ is/are allowed.

6) ☒ Claim(s) _1 and 2_ is/are rejected.

7) ☒ Claim(s) _3_ is/are objected to.

8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9) ☐ The specification is objected to by the Examiner.

10) ☒ The drawing(s) filed on _12 January 2004_ is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.

    Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

    Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

    a) ☒ All   b) ☐ Some * c) ☐ None of:

      1. ☒ Certified copies of the priority documents have been received.

      2. ☐ Certified copies of the priority documents have been received in Application No. _____.

      3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

    * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
    Paper No(s)/Mail Date _____.

4) ☐ Interview Summary (PTO-413)
    Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claims 1-3 are presented for examination.

Response to Arguments

Applicant's arguments filed August 6, 2004 have been fully considered but they are not persuasive.

Applicant, with reference to Cho et al. states that "... the correcting blocks in the third memory 130 and the fourth memory 140 are always error corrected by the error corrector 1 10 and then sent to the descrambler and error detector 1 12 . On the other hand, the present invention as claimed in claim 1 recites a second memory that has data stored therein after the data passes through a descrambling/error detection block which reads the data after error correction from a first memory, descrambles the data which has been subject to the error correction, and thereafter stores the data in the second memory, wherein when the data stored in the second memory are judged by the descrambling/error detection block as having no errors, the data stored in the second memory are transmitted to a host computer and when the data stored in the second memory are judged to contain an error, the data stored in the second memory are read out for each predetermined error correction block and subjected to error correction. It is apparent that, in Cho, there is no judgment as to whether or not the correcting blocks stored in the third memory 130 and the fourth memory 140 have errors before sending the correcting blocks to the error corrector 1 10. Instead, the correcting blocks are always sent to the error corrector 1 10 before

being transmitted to the descrambler and error detector 112." Although it is well

known in the art that if there are no errors detected, there is no need for

correction of nonexistent errors, the figure 3, element 108, receives the data from

the third and fourth memories. The 2-way arrow between 108 and 110, and the

one-way arrow between 108 and 112 in figure 3 (also figure 4) indicates direction

of the data.

Allowable Subject Matter

Claim 3 is objected to as being dependent upon a rejected base claim, but

would be allowable if rewritten in independent form including all of the limitations

of the base claim and any intervening claims.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35

U.S.C. 102 that form the basis for the rejections under this section made in this

Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published
under section 122(b), by another filed in the United States before the
invention by the applicant for patent or (2) a patent granted on an
application for patent by another filed in the United States before the
invention by the applicant for patent, except that an international
application filed under the treaty defined in section 351(a) shall have the
effects for purposes of this subsection of an application filed in the United
States only if the international application designated the United States
and was published under Article 21(2) of such treaty in the English
language.

Claims 1 and 2 are rejected under 35 U.S.C. 102(e) as being

anticipated by Cho et al. U.S. Patent No. 6,158,039.

As per claim 1, Cho et al. teach the claimed system having a descrambler

for restoring scrambled data in the process of encoding data, includes first and

second memories for correcting an error, and a memory controller for

transmitting error-corrected data to the descrambler while data read and

demodulated from the optical disk is written in one of the memories, and error-

correcting data written in the other memory while the demodulated and error-

corrected data is written and read. The system includes the steps of: alternatively

writing one error correcting block in the first and second memories upon

receiving demodulation data of one data sector including main data, inner parity

data and outer parity data, error-correcting a corresponding one error correcting

block; and reading error-corrected data from one of the first and second

memories when writing one error correcting block in the other one of the first and

second memories. After data is corrected it is transmitted to a host. (Abstract,

column 3 lines 20-54, column 4 lines 39-61, Figure 3)

As per claim 2, Cho et al. teach for the PI error correction of the first row,

data is read from a data region and data is read from a PI region to detect and

correct the error. The error-corrected data is again written in a position where

the error occurs. The PI error correction is performed with respect to both the

main data and PO. To calculate a syndrome, an error position and an error value

of one row, the data and parity are read by the unit of a word. Since the

maximum number of bytes per row which can correct the error is 10 bytes,

reading and writing are repeated by 10 times. PO error correction is performed in

the column direction by the unit of a byte, the memory should be accessed by the

unit of a byte. To calculate the syndrome, error position and error value of one

column, the data and parity are read. The maximum number of bytes per column

that can correct the error is 16 bytes. Error information detected from the

descrambler and error detector is stored in the second memory under the control

of a microprocessor memory access controller (FIG. 7, column 2 lines 42-49,

column 5 lines 61 through column 6 line 18)

Conclusion

Any inquiry concerning this communication or earlier communications from

the examiner should be directed to Cynthia Britt whose telephone number is 703-

308-2391. The examiner can normally be reached on Monday - Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the

examiner's supervisor, Albert Decady can be reached on 703-305-9595. The fax

phone number for the organization where this application or proceeding is

assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Cynthia Britt
Examiner
Art Unit 2133

GUY J. LAMARRE
PRIMARY EXAMINER